[0036] As shown in FIGS. 2 and 3, when the HIGH level of the pre-delayed clock is input to the input terminal 13a of the flip-flop 13 from the transfer clock circuit 6, the HIGH level of the delayed clock 0 is output from the output terminal 13c of the flip-flop 13, at a timing when the system clock input from the clock terminal 13b, makes a transition to the HIGH level. As the pre-delayed clock input to the input terminal 13a becomes the LOW level, the LOW level of the delayed clock 0 is output from the output terminal 13c, at a timing when the system clock input from the clock terminal 13b, makes a transition to the HIGH level. The delayed clock 0 is delayed for one pulse of the system clock, with respect to the pre-delayed clock.

[0037] As shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 0 is input to the input terminal 14a of the flip-flop 14 from the output terminal 13c of the flip-flop 13, the HIGH level of the delayed clock 1 is output from the output terminal 14c of the flip-flop 14, at a timing when the system clock input from the clock terminal 14b, makes a transition to the HIGH level. As the pre-delayed clock 0 input to the input terminal 14a becomes the LOW level, the LOW level of the delayed clock 1 is output from the output terminal 14c, at a timing when the system clock input from the clock terminal 14b, makes a transition to the HIGH level. The timing when the delayed clock 1 makes a transition to the HIGH level or to the LOW level is delayed for one pulse of the system clock, with respect to the delayed clock 0, and is delayed for two pulses of the system clock, with respect to the pre-delayed clock.

[0038] Also, as shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 1 is input to the input terminal 15a of the flip-flop 15 from the output terminal 14c of the flip-

flop 14, the HIGH level of the delayed clock 2 is output from the output terminal 15c of the flip-flop 15, at a timing when the system clock input from the clock terminal 15b, makes a transition to the HIGH level. As the pre-delayed clock 1 input to the input terminal 15a becomes the LOW level, the LOW level of the delayed clock 2 is output from the output terminal 15c, at a timing when the system clock input from the clock terminal 15b, makes a transition to the HIGH level. The timing when the delayed clock 2 makes a transition to the HIGH level or to the LOW level, is delayed for one pulse of the system clock, with respect to the delayed clock 1, and is delayed for three pulses of the system clock, with respect to the pre-delayed clock.

[0039] Similarly, as shown in FIGS. 2 and 3, when the HIGH level of the delayed clock 2 is input to the input terminal 16a of the flip-flop 16 from the output terminal 16c of the flip-flop 15, the HIGH level of the delayed clock 3 is output from the output terminal 16c of the flip-flop 16, at a timing when the system clock input from the clock terminal 16b, makes a transition to the HIGH level. As the pre-delayed clock 2 input to the input terminal 16a becomes the LOW level, the LOW level of the delayed clock 3 is output from the output terminal 16c, at a timing when the system clock input from the clock terminal 16b, makes a transition to the HIGH level. The timing when the delayed clock 3 makes a transition to the HIGH level or to the LOW level, is delayed for one pulse of the system clock, with respect to the delayed clock 2, and is delayed for four pulses of the system clock, with respect to the pre-delayed clock.